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FIG.1
PRIOR ART

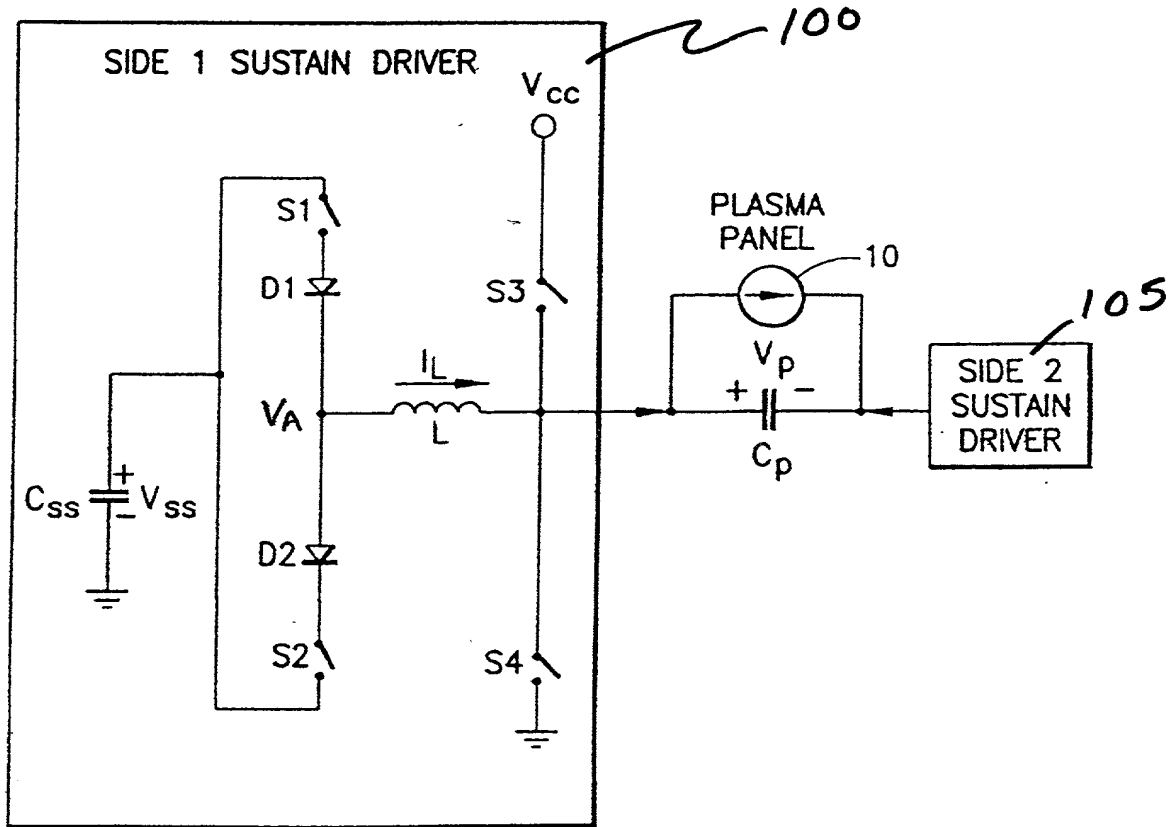
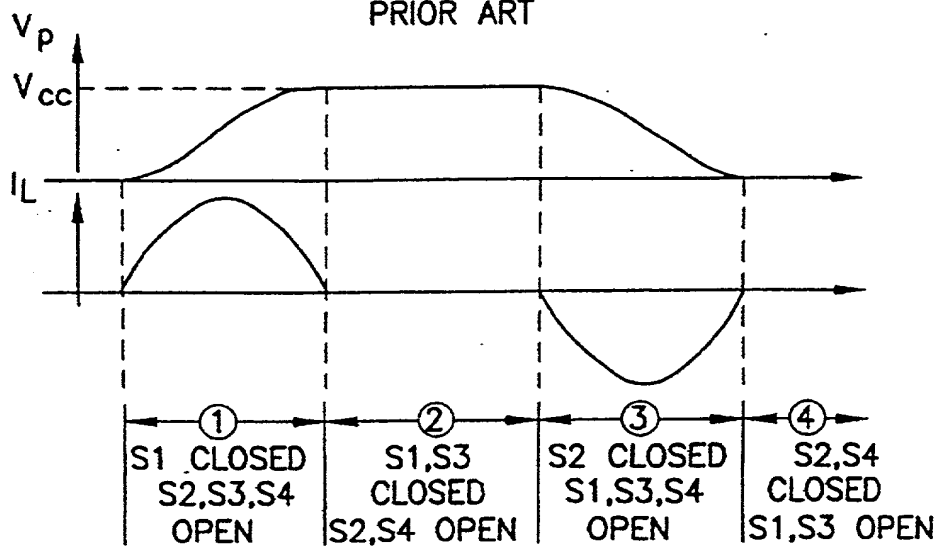


FIG.2
PRIOR ART



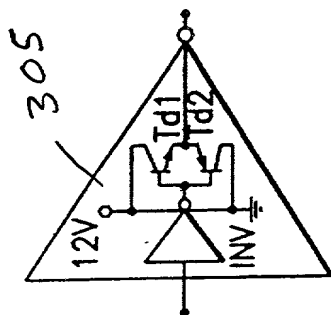


FIG. 3

PRIOR ART

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STATE

1

2

3

4

SOURCE
12

5V

0V

NODE V1

V_{SS}

0V

NODE V2

V_{CC}

V_{SS}

NODE
A

V_{CC}

V_{SS}

0V

V_p

V_{CC}

V_{SS}

0V

I_L

(+)

0A

(-)

VG3

V_{CC}

V_{CC}-12

VG4

12V

0V

t1 t2

t3

FIG 4

PRIOR ART

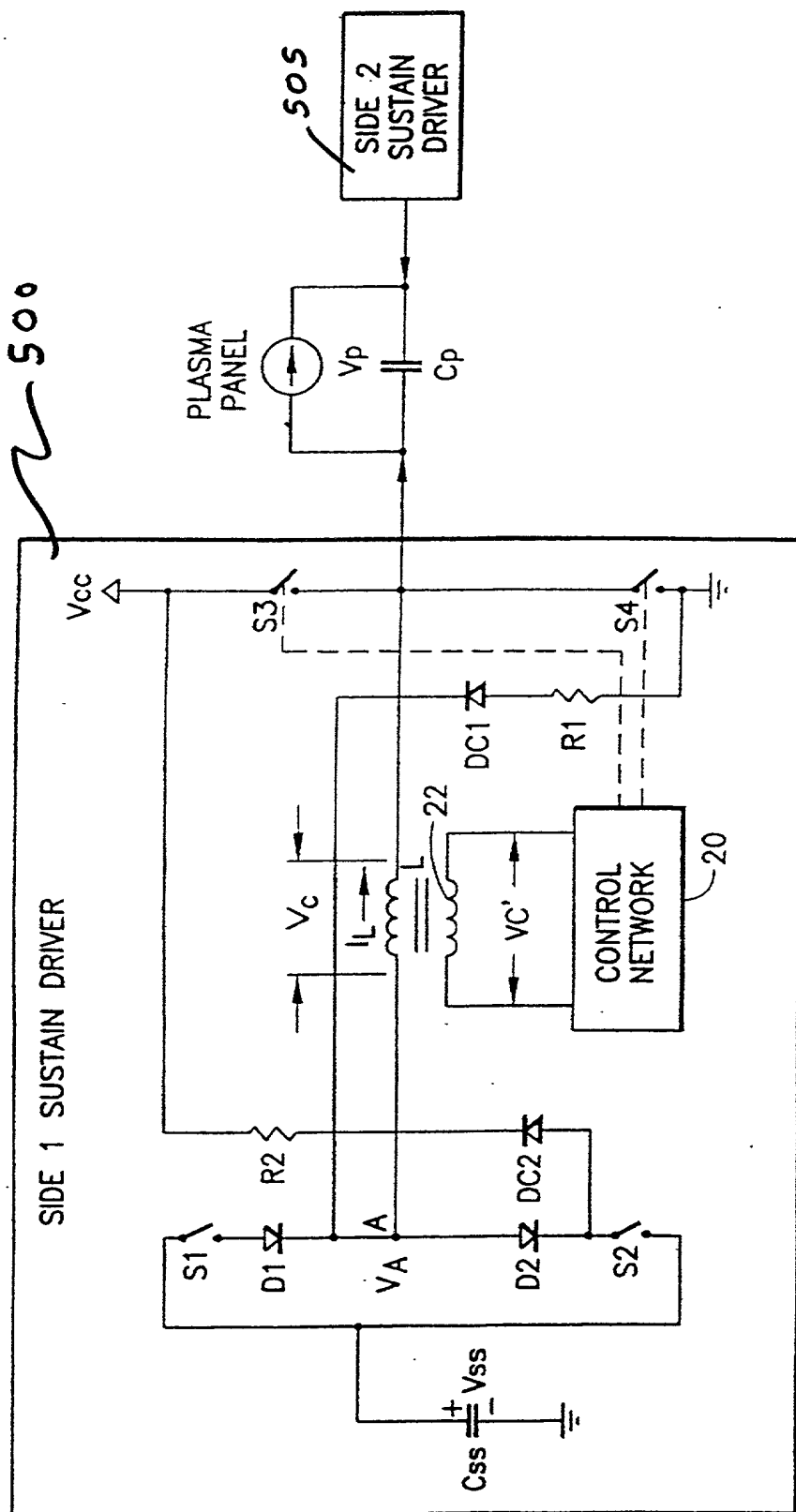


FIG. 5
PRIOR ART

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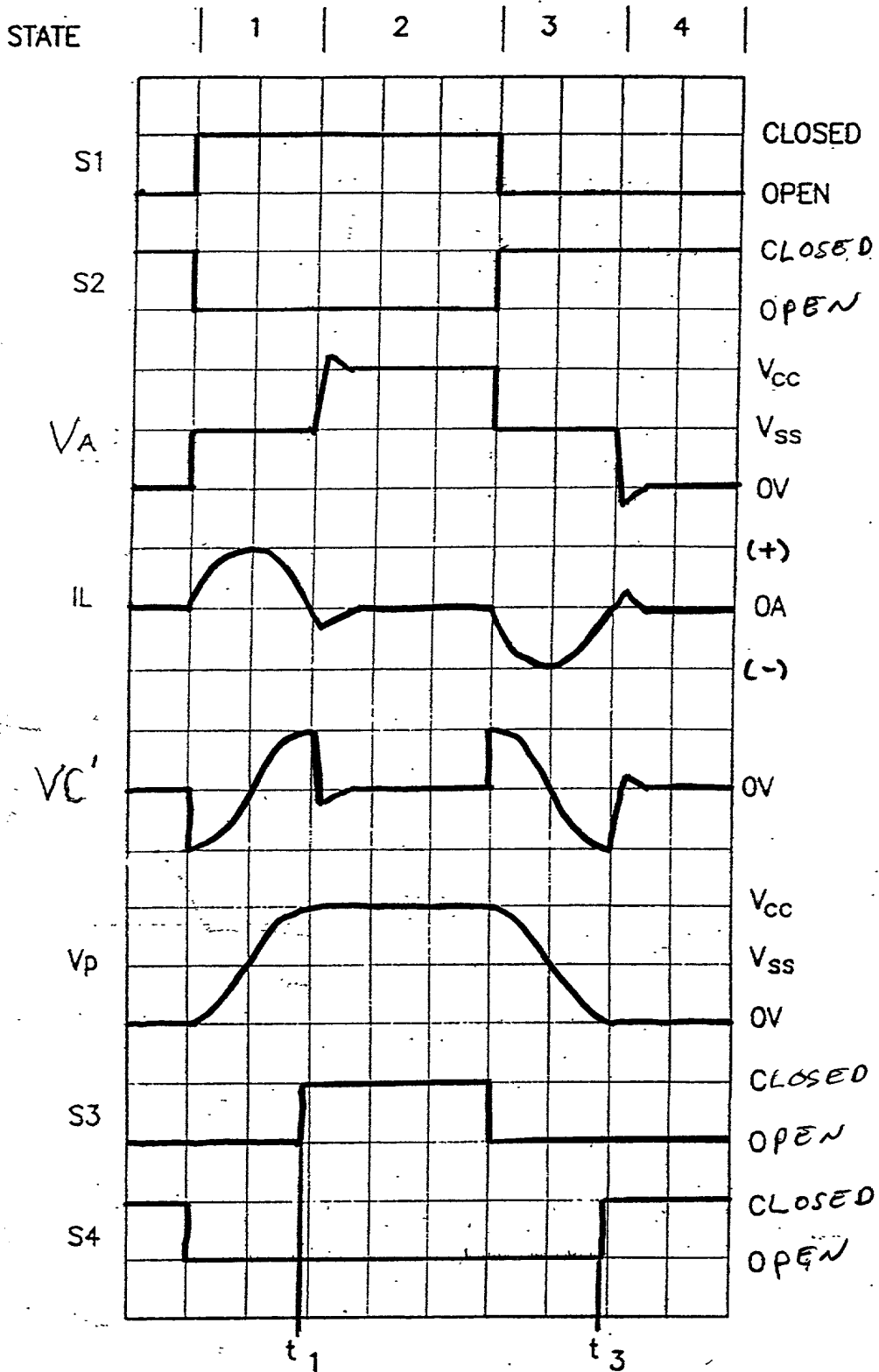
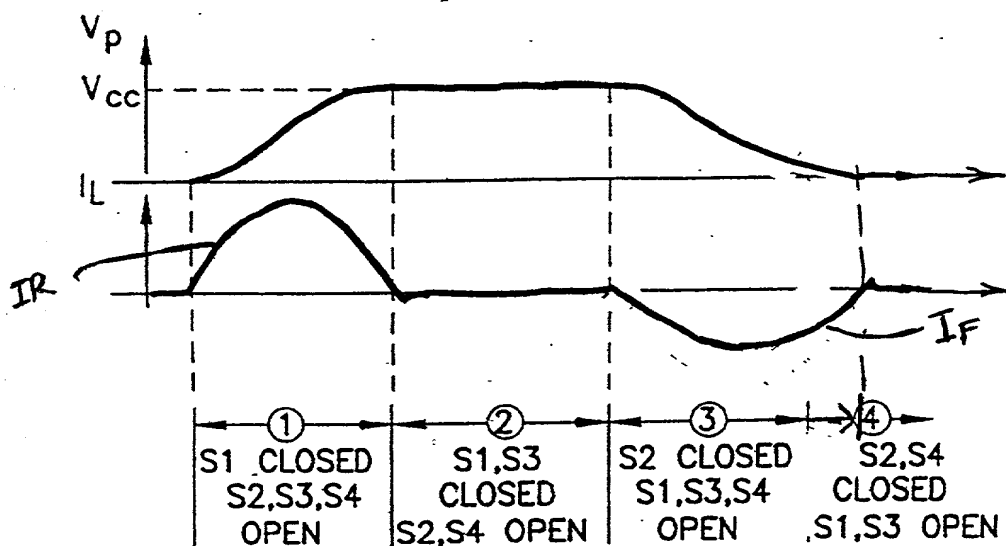


FIG. 16
Prior Art

FIG. 7



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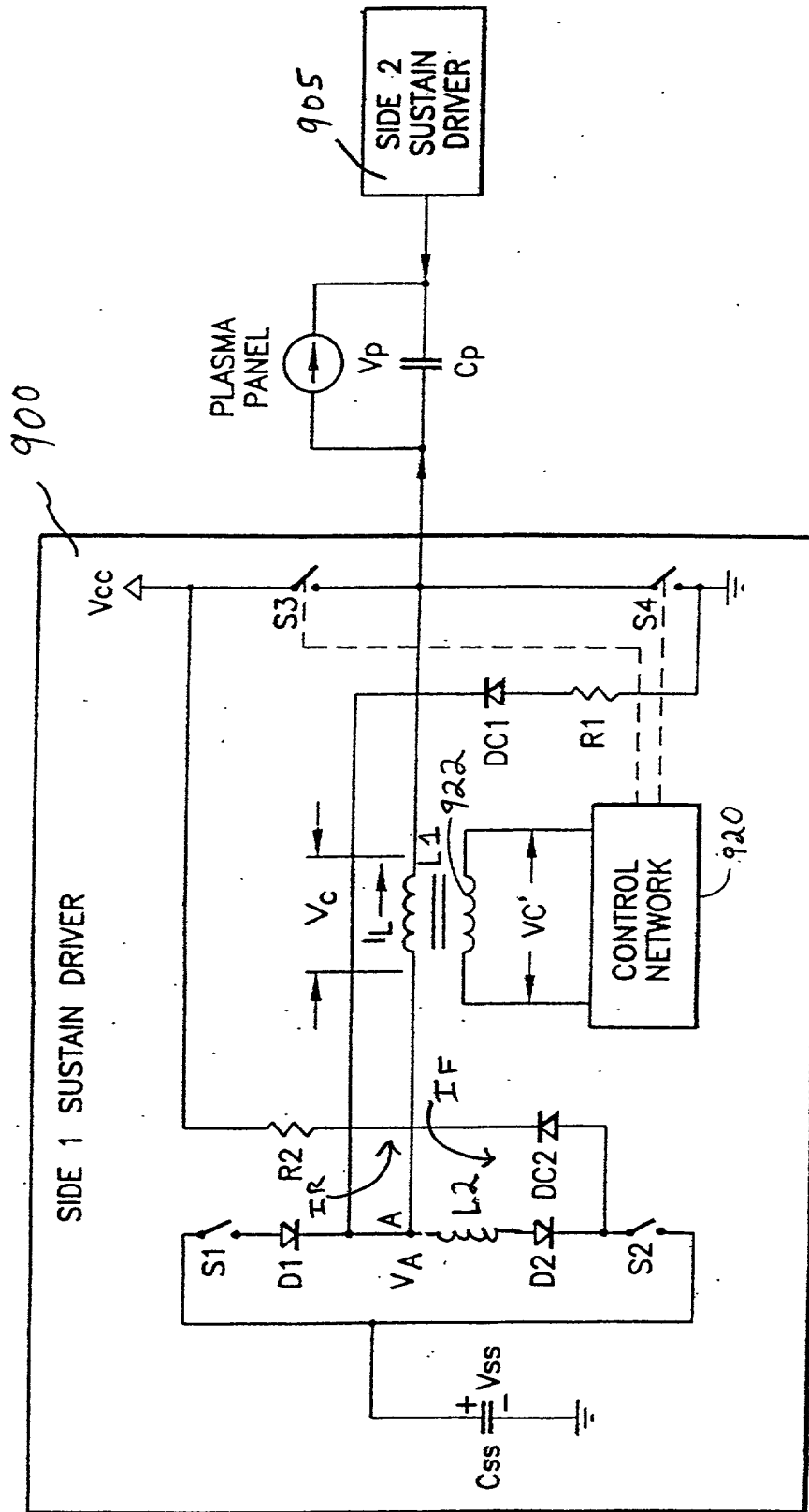


FIG. 9

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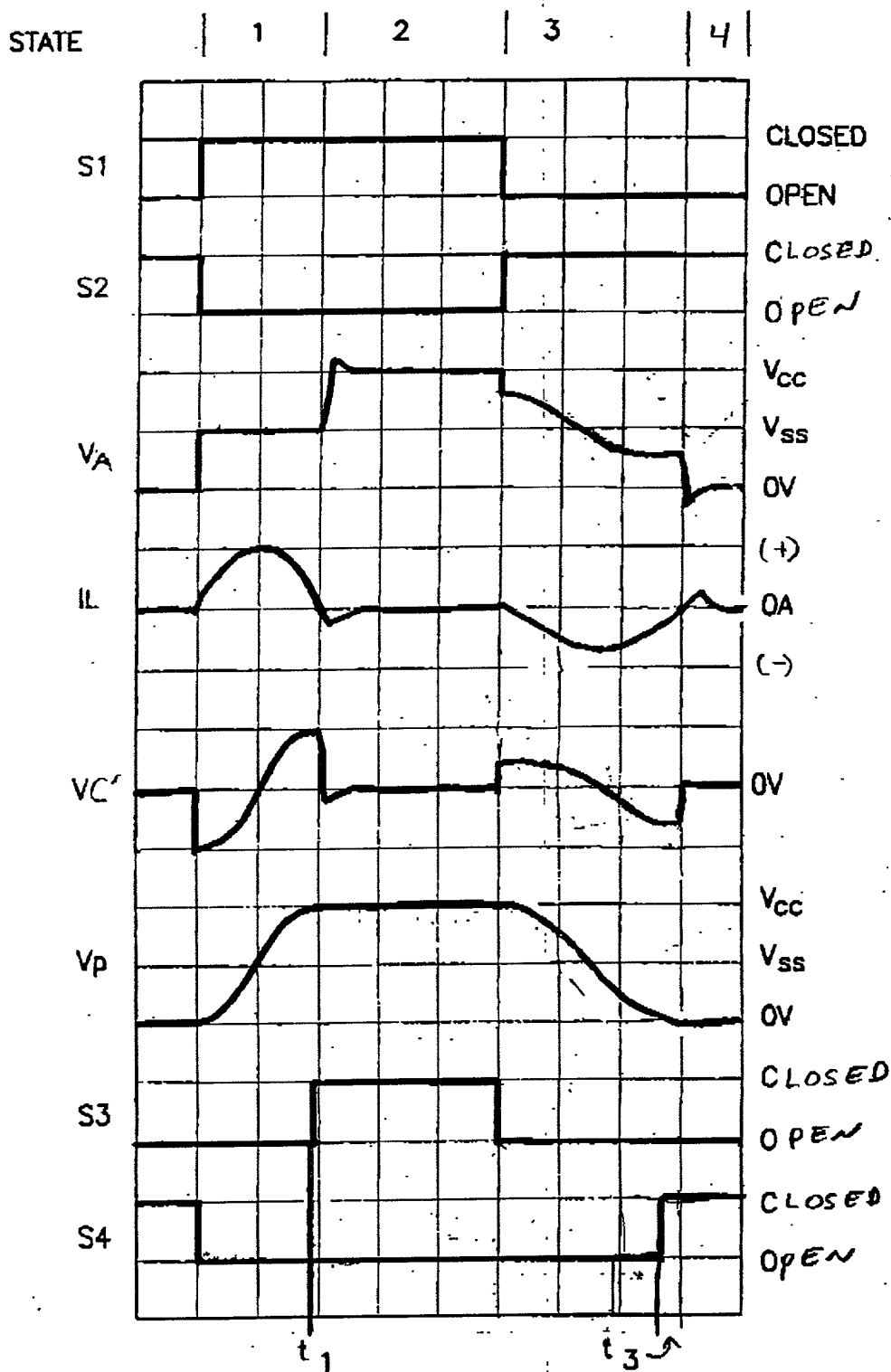


FIG. 10

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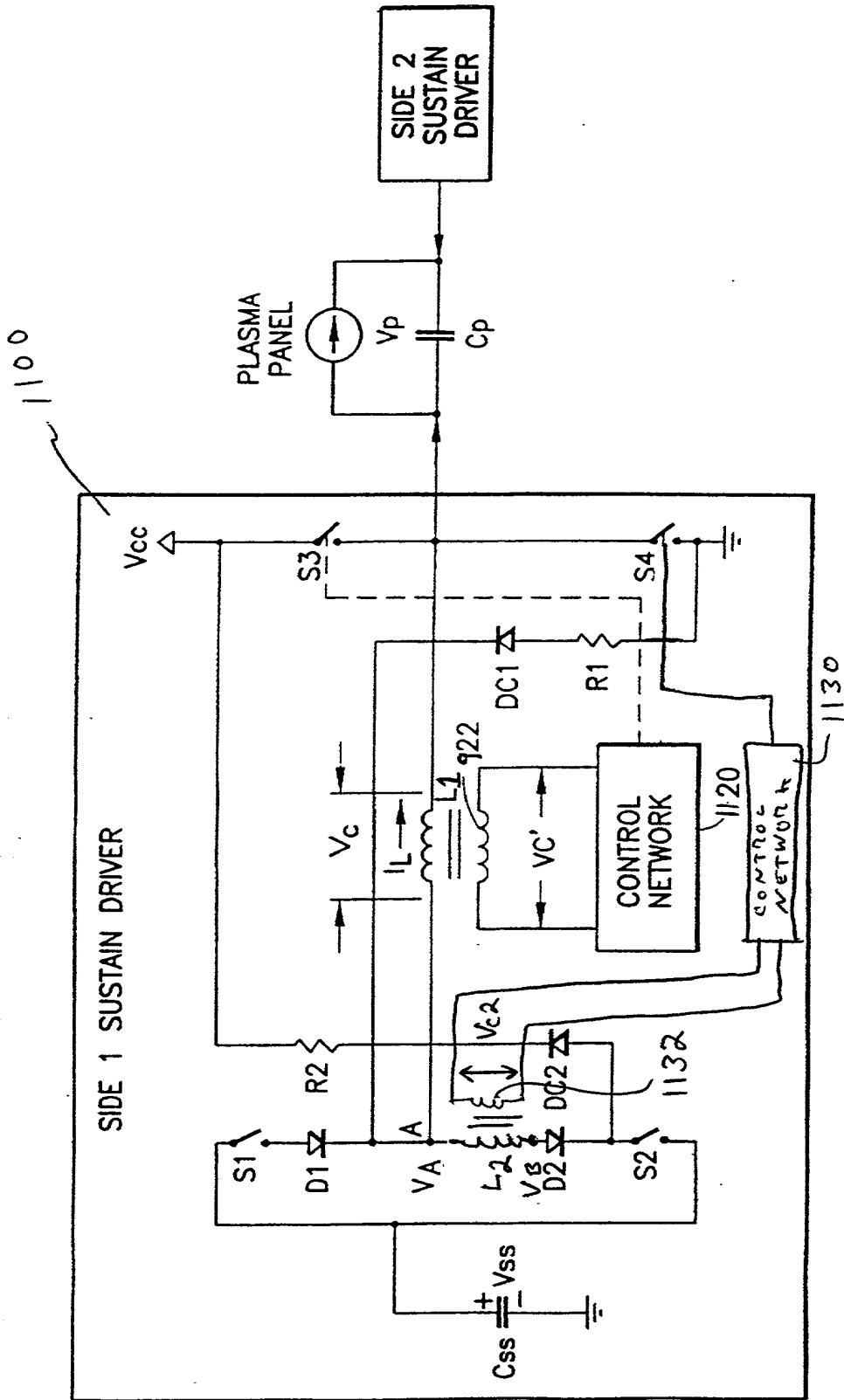


FIG. 11

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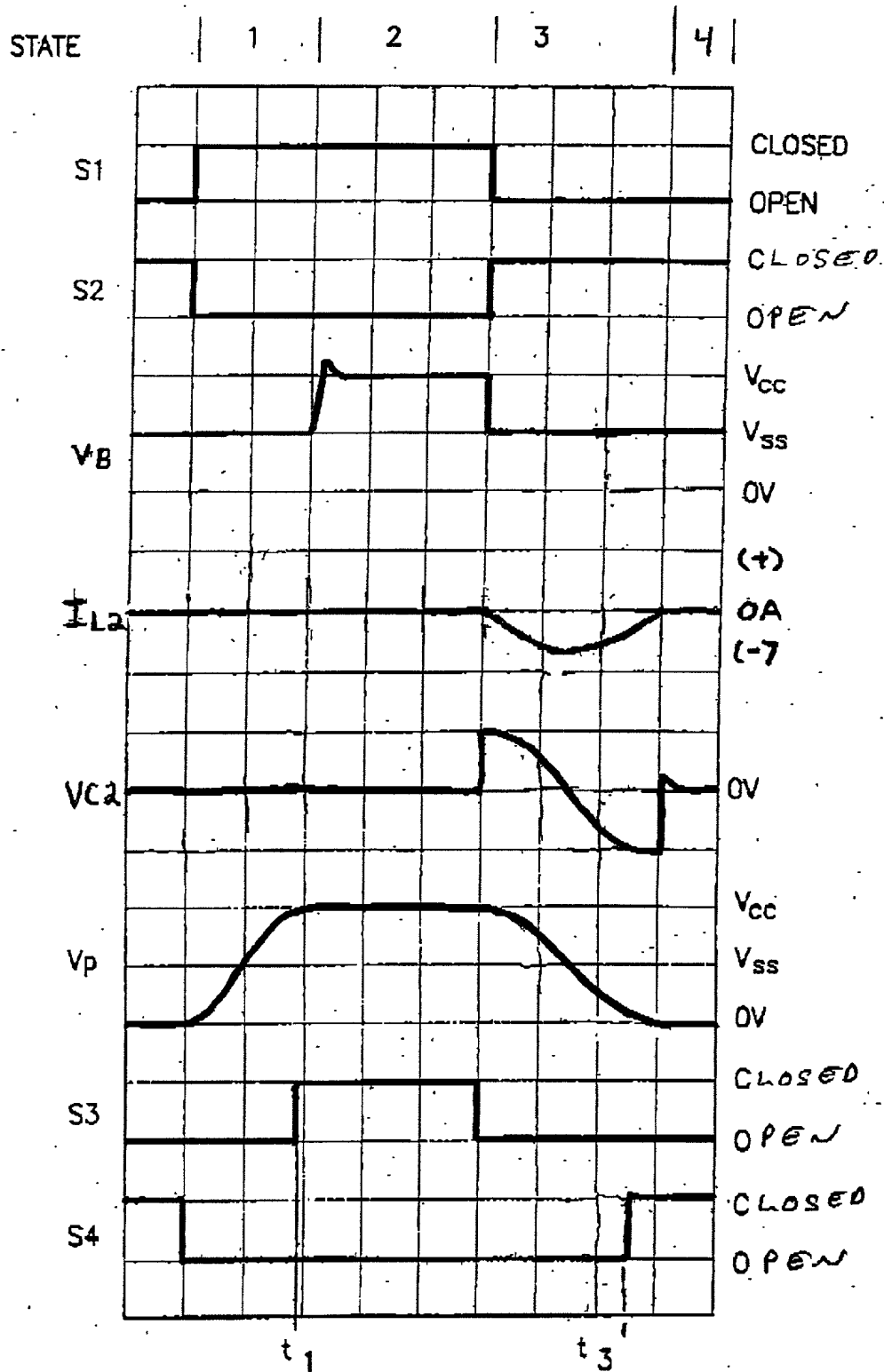


FIG. 12

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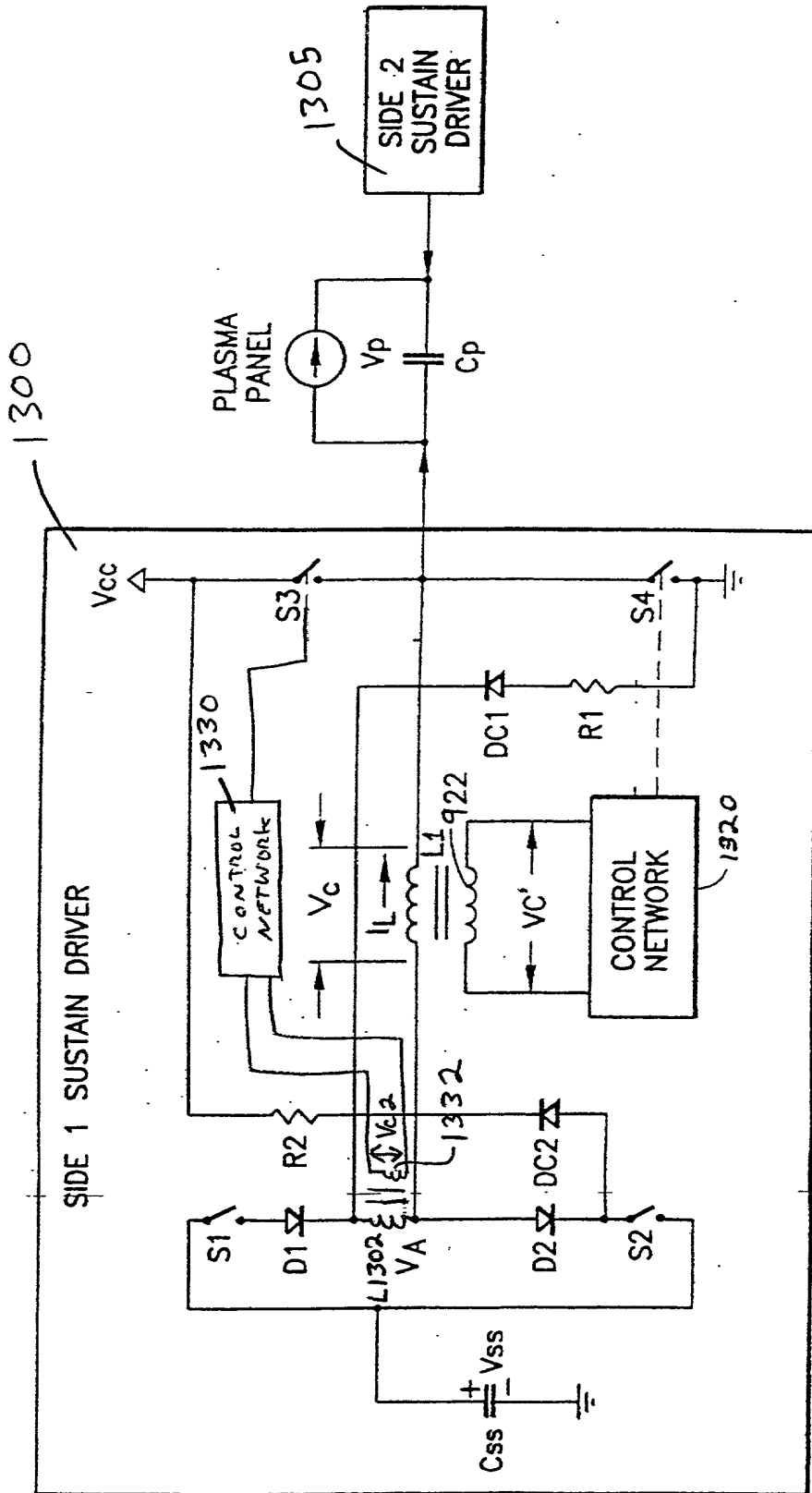


FIG. 13

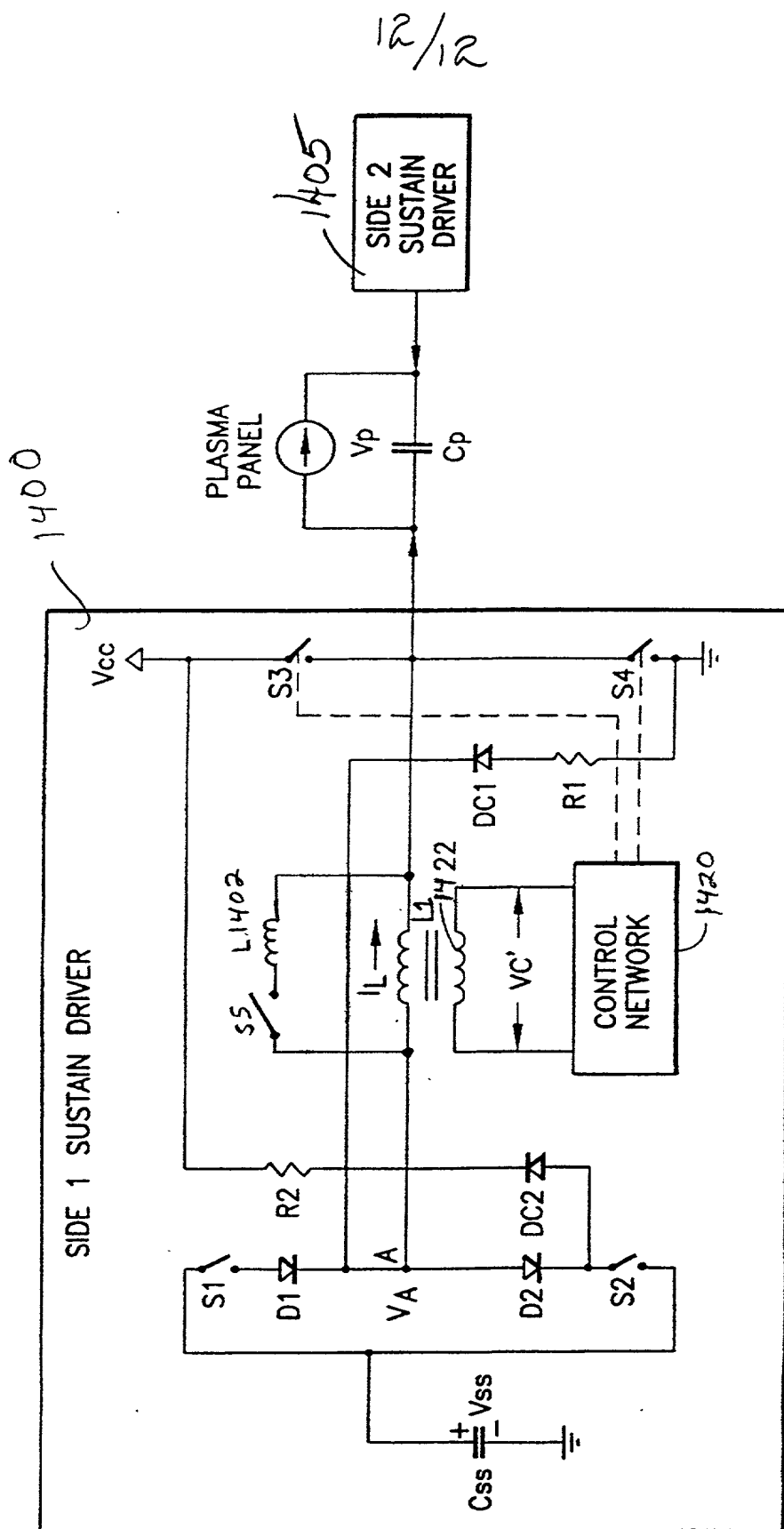


FIG. 14.